IN THE SPECIFICATION

Please amend the specification as follows.

[0033] An adhesive, such as a solder, may be positioned on the upper surface 420a of the lead frame pad 420 to adhere the semiconductor chip 440 to the lead frame pad 420. However, the lower surface 420b of the lead frame pad 420 ~~is directly bonded to~~ directly contacts the upper surface 410a of the ceramic layer 410 without an adhesive. In other words, the lead frame pad 420 ~~is bonded to~~ contacts the ceramic layer 410 by using the molding material 450. When manufacturing the discrete package 600, a soldering process is not performed between the ceramic layer 410 and the lead frame pad 420. Thus, there is no need to form a conductive layer pattern on the upper surface 410a of the ceramic layer 410 for the soldering process. Since the discrete package 600 uses the bare ceramic layer 410 (which can be fabricated at a cost of about three times less than a ceramic layer coated with a conductive layer pattern) as an insulating heat sink, the present invention is able to reduce the manufacturing costs. The ceramic layer 410 is also cheaper than using a DBC substrate, which is itself more expensive than the ceramic layer coated with the conductive layer pattern. Also, the thermal transfer efficiency of the discrete package 600 is higher than that of the discrete package 300 which is insulated using a portion of a molding material. In general, a semiconductor package containing EMC with a filler of 80 wt% (which is used as a molding material) has a thermal transfer efficiency of 2.09 W/m°C at a temperature of about 25°C. A semiconductor package contains a ceramic layer (made of Al_2O_3 with 96 degree of purity) has a thermal transfer efficiency of 27 W/m°C at a temperature of about 25°C.